## **Breakdown Voltage Improvement and Analysis of GaN HEMTs through Field Plate Inclusion and Substrate Removal**

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**Extensive studies have concluded that breakdown mechanisms in gallium nitride (GaN) high electron mobility transistors (HEMT) can be improved by substrate reduction and the addition of field plate (FP) on their schematics. A comprehensive physics-based (PBM) model of a common HEMT provides the base comparison to conduct the aforementioned analyses but more specifically to study different geometric FPs. The electric field distribution across the source, gate, and drain is analyzed for each geometric case in order determine the breakdown voltage (BV) origin as well as their I-V characteristic curves.**

*Index Terms***—GaN, HEMTs, physics based modeling, finite element analysis, wide band gap devices.** 

## I. INTRODUCTION

RANSISTORS based on GaN material are extremely promising devices in the area of microwave circuits and power systems because its material properties such as high peak electron velocity, saturation velocity and thermal stability. Theoretical  $r_{on}$  – BV limits for lateral HEMT are better than Vertical GaN (VGaN) devices as the mobility of electrons in the twodimensional electron gas (2DEG) is higher than the mobility in the VGaN [2]. Notwithstanding, HEMTs are sensitive to surface breakdown and are not easy to scale to higher power. Therefore, there is a need to study the BV mechanism of the HEMT and the ways to increase it. The BV mechanisms are: source-drain breakdown (punch-through), gate-drain breakdown (leakage through the Schottky diode), vertical breakdown (poor compensation of the buffer layer) and impact ionization (an electronhole pair generation close to the gate) [3]. The latter depends on the critical electric field  $(E_{crit})$  of the material, or the field strength required to initiate impact ionization causing an avalanche breakdown [4]. T

There are 2 ways to avoid the BV: ensuring that the electric field is smaller than the  $E_{crit}$  at the operating point of the HEMT or enlarging the drift distance. The drift distance is held constant as a constraint, thus, the only solution available is to redistribute  $E_f$ . Three solutions have been suggested in literature in an effort to improve the BV: a variation of the passivation material, changing the substrate material, and the application of a FP structure on either the source or gate [5]. Reference [6] proposed the etching of the silicon (Si) substrate which resulted in a significant increase in the BV. Following the same idea, we propose to study the progressive etching of the Si substrate to obtain the optimum Si thickness that results in a higher BV. Subsequently, a FP investigation is conducted with diverse structures. The different FP configurations are depicted in Fig. 1 where 2 types of FP are noted: source FP (S-FP) and gate FP (G-FP). Additionally, two different S-FP are studied as shown in Fig. 1(b) and (c). The studies performed in this article are based on PBM that can provide us with a specialized set of tools based on the geometry, materials, and physics of HEMT to evaluate mechanisms that can increase the BV [7], [8].

TABLE I. GAN-FET DESIGN PARAMETERS AND CASES OF STUDY





Fig. 1: Schematic layer structure (a) Base (b) S-FP1 (c) S-FP2 and (d) G-FP3.

VARYING THICKNESS OF THE SILICON SUBSTRATE In the first study, multiple etching depths of the Si substrate are performed in the structure shown in Fig. 1(a). Dimensions of the HEMT under study are as shown in Table I, where initially a silicon dioxide (SiO2) passivation layer is used as well as a 13.98 µm Si substrate thickness. This thickness is then reduced in 1 µm steps terminating at 0.98 µm where the BV progression is shown in Fig. 2. From this study, the optimum substrate is identified to be is 2.98 µm and is used for each of the FP cases. The BV on Fig. 2 are calculated by developing the I-V characteristic curve for each of the etched cases by finding their maximum slope. The HEMT is swept in off-state ( $v_a = -2V$ ).



Fig. 2: BV against the Si substrate thickness for the etching reduction. III. COMPARATIVE RESULTS AMONG ALL STUDIED CASES

The structure in Fig. 1(a) is then modified to evaluate the BV performance with the application of different FP configurations and a modified passivation material. The BV progressions (Fig. 3(a)) and electric field  $E_f$  distribution at 2 heights ( $y_2 =$ 0.721  $\mu$ m surface of the device and  $y_4 = 1.02 \mu$ m 2DEG channel) along the x axis have been conducted at  $V_{ds} = 610 \text{ V}$ which is the smallest BV for the original case (Fig. 4).

First, substrate etching of the original to the optimal thickness results in a dramatic increase of the BV by 226.3 V. Two S-FP architectures are then tested as modifications to the optimal Si substrate thickness case. A two-part staircase S-FP1 as shown in Fig. 1(b) results in an immediate 30 V increase of the BV. The SiO2 passivation layer is then replaced with Silicon Nitride (SiN) resulting in a further increase of 14V. Next, an alternative single part S-FP architecture (FP2) is evaluated as shown in Fig. 1(c) keeping SiN as the passivation layer which results in a slight drop in the BV versus FP1. However, it should be mentioned the BV is only around 5V lower with a potential trade-off in easier fabrication of a single-part structure. A summary of the results are shown in Table II.

Next, a single-part G-FP structure (FP3) is evaluated as depicted in Fig. 1(d) which results in almost the same performance as FP1. Fig. 3(b) demonstrates the origin of the BV for the optimal Si substrate thickness case (FP1 with SiN passivation) which points toward drain-source sub-threshold leakage [3]. From Fig. 4(a) and Table II, it can be noted that as  $E_{fmax}$  decreases the BV increases in all the cases (as expected). However,  $E_{fmax}$  is the highest for the FP1-SiN device which appears to be contradictory. This can be explained noticing that this  $E_{fmax}$  is located at  $x = 0.5 \mu m$ , at the end of the S-FP contact and separated from the 2DEG by the SiN passivation layer with very high dielectric strength of 10MV/cm. From Fig. 4(b), which corresponds to the cross section along the 2DEG, it is clear that the  $E_{fmax}$  of the FP1-SiN is the minimum.





IV. ANALYSIS OF THE BEST CASE WITH FIELD PLATE

For the best FP case, the  $E_f$  distribution along the *x*-direction at 4 different heights (at  $BV = 880.61 \text{ V}$ ) is shown in Fig. 5 and also as a 2D map in Fig. 6. Fig. 5 shows the key advantage of the FP layout as it redistributes the field and relocates the peak electric field along the *x* and *y* plane keeping it below the critical value and hence increasing the BV. The same behavior is more clearly observed in Fig. 6(b). It is shown that the highest field strength is present right at the corner of the FP-SiN interface on the drain side of the gate at 14.9 MV/cm.<br>V. CONCLUSION

In this article it is demonstrated that the Si substrate reduction plus the addition of field plate improve the BV in classical HEMTs. In the full version of the article, we will present more FP cases such as the dual and double plus an analytical study of the FP effects of the HEMTs.









Fig. 6: 2D electric field distribution for the case of the FP1. (b) zoom

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